

Lock-in-Thermography for 3- dimensional localization of electrical defects inside complex packaged devices

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Abstract

It has been shown that microscopic Lock-in-Thermography (LiT) can be used for localization of electrical active defects like shorts and resistive opens in integrated circuits. This paper deals with the application of LiT for non-destructive failure analysis of fully packaged single and multi chip devices. In this case inner hot spots generated by the electrical defects typically can not be imaged directly because the mold compound or adhesives above are not IR transparent. Inner hot spots can only be detected by measuring the corresponded temperature field at the device surface. By means of failed and test devices will be shown, that LiT is sensitive enough to measure such temperature fields. In addition to the lateral localization of inner hot spots its depth can also be determined by measuring the phase shift between the electrical excitation and the thermal response at the device surface. Furthermore, the influence of the lock-in-frequency and mold compound thickness to lateral resolution and signal to noise ratio will be discussed. Using real failed single chip and stacked die devices two analysis flows were demonstrated to locate inner defects.

Introduction

Modern system in package (SiP) or package on package (PoP) devices are getting more and more complex. Therefore, the localization and analysis of electrical defects inside such a complex three dimensional built up can be difficult and time consuming. Especially for this kind of devices methods are required which are able to detect defects in a non-destructive way because every preparation step can effect the failure mode or destroy the overall functionality of the device. Additionally, in multi chip devices electrical active structures, like ICs or

interconnects are often vertically stacked. Therefore defect structures are covered by surrounded materials. Only the upper chip level can be investigated using standard failure localization techniques like OBIRCH [1], liquid crystal thermography [2], or emission microscopy after removing the mold compound by opening the device. Lower chip- or interconnect levels can not be investigated by this methods in a non-destructive way... Furthermore, assumed shorts between bond wires could be removed by etching the mold compound. In such cases only non-destructive-testing methods are necessary to localize defects. There are only several, very specific methods known satisfying these requirements. Time domain reflectometry (TDR) can be used finding the failure site by measuring the delays of electrical signals. Magnetic microscopy [3] uses the fact that every current flow generates a local magnetic field, which is not affected by the surrounding material. It will be shown that LiT can also be used for non-destructive testing, measuring the corresponding temperature fields at the device surface caused by inner hot spots.

As shown in literature, the method of LiT is a sensitive and easy to handle method for hot spot detection on chip level. [4], [5], [6]. The defect is stimulated electrically by a periodically pulsed supply voltage which produces a periodically thermal response. This response is detected by a free-running IR camera and is split into an in-phase-part and an out-of phase-part related to the excitation signal by using two correlation functions. From these basic signals the amplitude and the phase signal of the thermal response can be calculated:

$$amplitude = \sqrt{(S^{in-phase})^2 + (S^{out-of-phase})^2}$$

$$phase = \arctan \frac{S^{out-of-phase}}{S^{in-phase}}$$

Using these two signals, the main advantage to the steady state thermography can be seen clearly. Due to the periodically pulsed excitation the heat spreading and therefore the thermal blurring is lateral limited which is direct related to the lock-in-frequency. In addition, due to the lock in amplifier principle the detection limit is improved by the 3-4 orders compared to the steady-state-thermography. Nevertheless, the phase signal contains information about the time delay between electrical stimulation and thermal response. This phase shift is influenced by thermal spreading inside the mold compound or adhesives and can be used for three-dimensional defect localisation. the basic principle is explained in Figure 1.

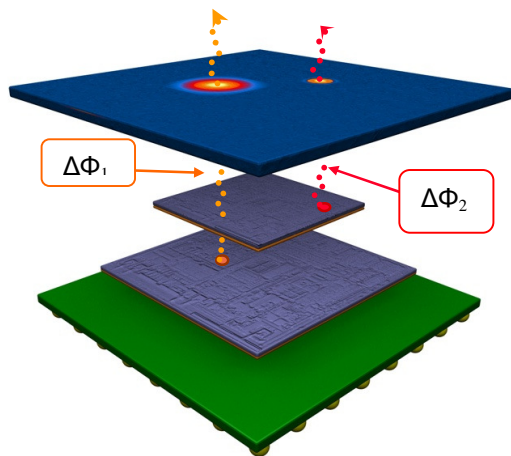


Figure 1: Sketch of the heat expansion in an excited device. Depending on the depth of the defect a phase shift $\Delta\Phi$ between excitation and detection occurs due to heat conduction through the layer system.

Typically, the mold compounds or adhesive materials are not IR transparent. Therefore inner hot spots generated by electrical defects can not be imaged directly. But inner hot spots can be detected by corresponded temperature field at the device surface. Heat flow is a time-depending process. Therefore, a phase shift $\Delta\Phi$ between excitation and detection of the local heating occurs depending on the depth of the defect and the thermal behaviour of the material. Visa versa, by measuring the phase shift the depth of the defect can be determined. The phase shift value depends mainly on heat conduction, heat capacity and thickness of each layer above an inner heat source at the defect site.

Experimental

1. Two dimensional defect localization in fully packaged single chip device

A fully packaged single chip device with a local inner short acting as a point heat source was used to demonstrate the potential of the LiT for non-destructive failure localization. LIT measurements were done using supplied voltage of 0.4 V,

a current of 4.17mA and a measuring time over 5000 periods. The lock-in-frequency was varied starting at 3 Hz up to 12 Hz. As it can be seen from figure 2, a relatively large hot spot at the surface could be detected using a low excitation frequency (3Hz) due to thermal spreading. This spot size can be reduced by increasing the lock-in-frequency.

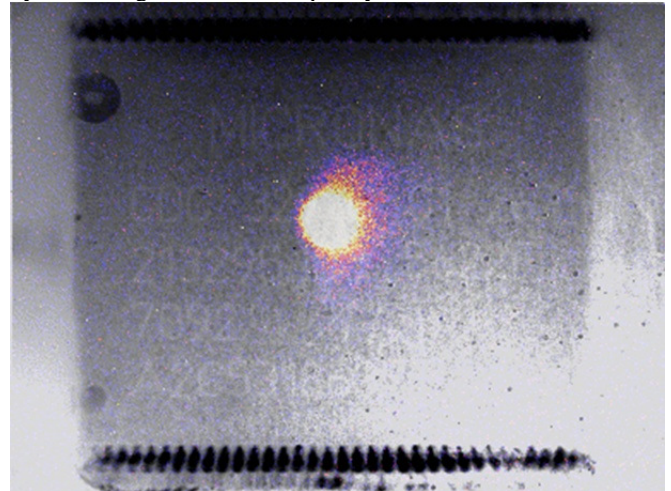


Figure 2: Hot spot detection in a fully packaged device using a lock-in-frequency of 3Hz. Phase and topography image were overlaid. .

Increasing the lock-in-frequency to 6 Hz reduces the spot size at the surface significantly and allows a better localization of the hot spot (Fig.3). On the other hand, the signal-to-noise-ratio is significantly reduced. Further increasing of the lock-in-frequency leads to the point that the hot spot can not be detected on the surface in relevant measuring times.

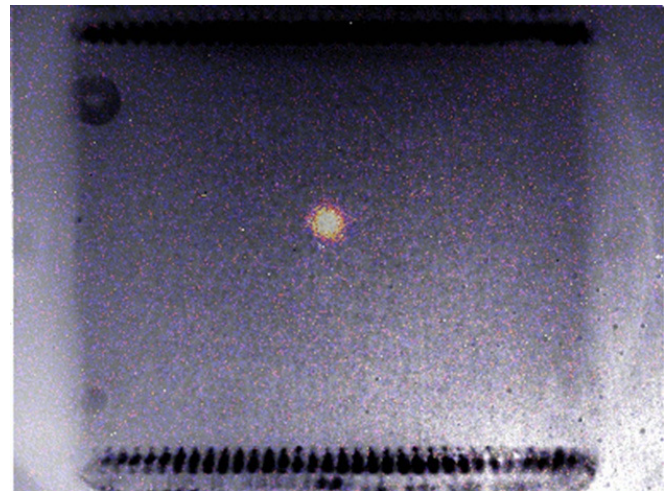


Figure 3: Hot spot detection in a fully packaged device using a lock-in-frequency of 6Hz. Phase and topography image was overlaid.

As a second way, in order to reduce thermal spreading, the thickness of the mold compound above the failure can be reduced. This could be done using a local grinding tool, Fig. 4. A second fully packaged single chip device with an inner short was investigated by LiT. The inner hot spot was excited using a supply voltage of 0.4 V at 2 Hz frequency leading to a

current of 2.61mA. It can be seen from figure 5 that a hot spot was located outside of the chip. After reducing the thickness of the mold compound a second LiT measurement was done using a higher LiT frequency of 16.5 Hz. It can be seen from figure 6 that this leads to the result that the hot spot size is strongly reduced compared to the first measurement (Fig.5).

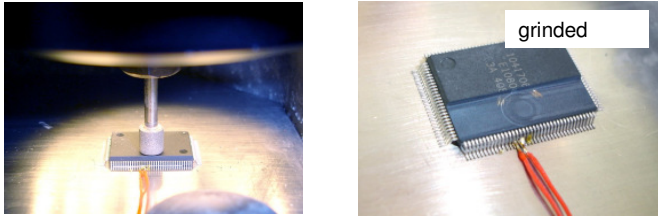


Figure 4: Reducing the thickness of the mold compound by local mechanical grinding.

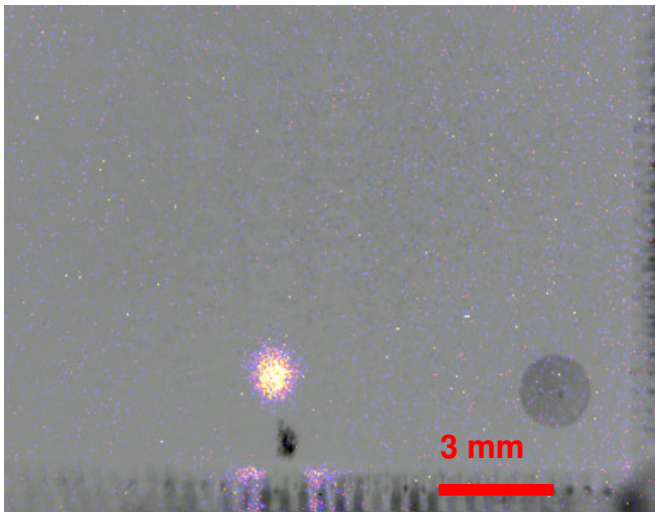


Figure 5: Hot spot detection by LiT at a fully packaged device. Shown is the overlay of amplitude and topography image.

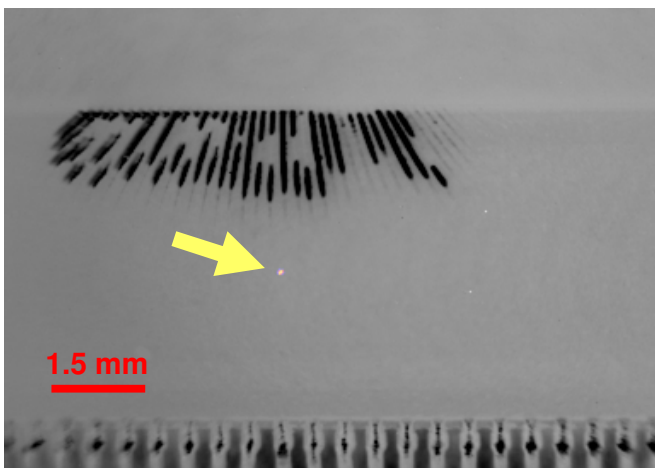


Figure 6: Second LiT measurement after reducing the mold thickness above the short defect. Shown is an overlay of amplitude and topography image.

As a result of the reduced thickness and the resulting increase of the spatial resolution the hot spot could be located between two adjacent bond wires. After additional target preparation by

mechanical cross sectioning the root cause of short path could be found as a metal splinter by light and scanning electron microscopy investigations, seen in Fig. 7.

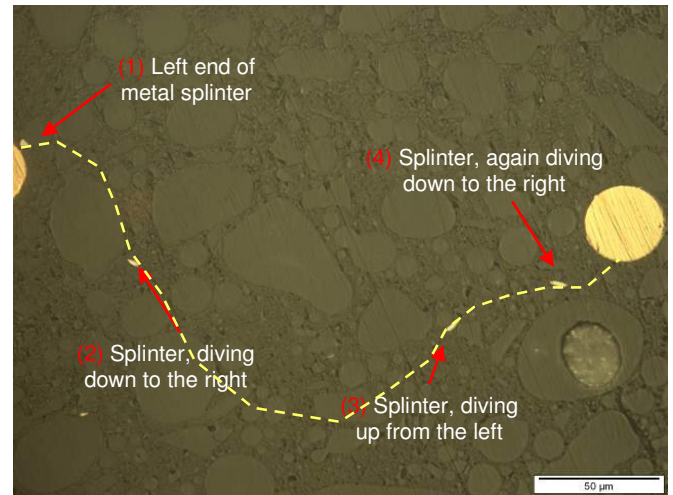


Figure 7: root cause after target cross sectioning: metal splinter between adjacent bond wires

2. Three dimensional defect localization at a fully packaged stacked die device

2-dimensional non-destructive failure localization at single chip devices can be used to divide between chip- or interconnect-defects, which is important for further failure analysis steps. The 3-dimensional failure localization is helpful, if separate chips were stacked on top of each other. In this case the non-destructive localization of the defect allocated to the chip- or interconnect level can strongly reduce failure analysis time. An easy failure analysis flow at a defective stacked die device is subsequently shown. The multi chip device contained two stacked ICs. The inner short was excited by a supply voltage of 0.5V and a current of 8.02mA. The LiT was done using a lock-in-frequency of 2Hz. As it can be seen from Figure 8 a hot spot in the area of the IC stack was found.

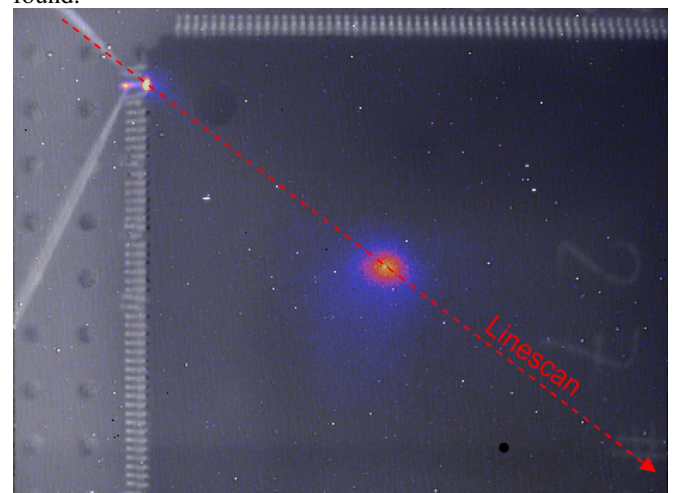


Figure 8: LIT phase image of a fully packaged stacked die device with inner short. The dotted line shows the position of the linescan determining the phase shift.

After the first LiT measurement, the mold compound above the upper chip was removed by local mechanical grinding and chemical etching. Then a second LiT-measurement was done. As it can be seen from Figure 9, the hot spot size is strongly reduced. Due to the point that both stacked chips contain electrical active structures in the area of the hot spot the short could be located at the upper or lower chip.

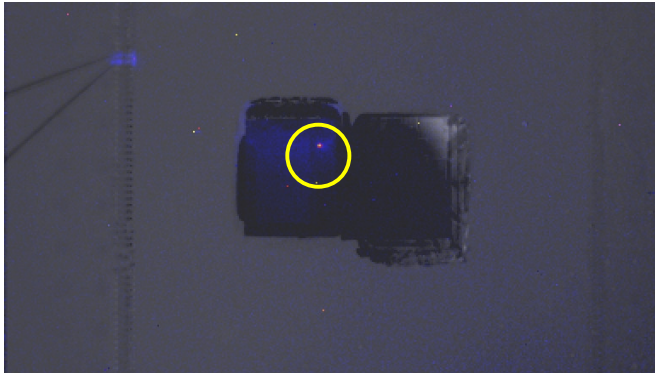


Figure 9: LiTimage after removing the mold compound.

As a subsequent step, the upper chip level was de-contacted by removing the bond wires. The following electrical and LiT-measurements lead to same results. In conclusion the short defect is situated on the lower chip level. Because of the IR-transparency of the chip material (mainly Si) the thermal defect on the lower chip could be imaged through the upper chip.

This procedure can be extended to multi chip stacks with separately operating chips. More complicated is the case if the chip functionality depends from each over or the defect occurs at the interconnect level. Therefore, an all-encompassing method to allocate the defect vertically is necessary. This could be done in a non-destructive way using LiT and its opportunity of measuring the phase shift generated by time-depending heat flow.

In order to demonstrate this, a linescan through the detected hot shots in the phase image of the fully packaged device was taken, which can be seen in figure 8. Figure 10 shows the resulting graph of the linescan where two phase signals can be regarded. The left one, marked black, comes from the contact needles of the supply voltage and the other one, marked red, is the phase shift occurring by the defect.



Figure 10: Graph of the linescan. The phase shift on the left side (marked black) occurs from the electrical contact, the phase shift marked red comes from the defect.

It has to be noticed that the phase has an amount of 360° at the device surface and therefore the resulting phase is calculated by:

$$|\Delta\Phi| = |\Phi_{measured} - 360^\circ|$$

which leads to a phase shift of 30° for the contact needles and 140° for the defect. The difference between both is 110° . This phase shift could be used to recalculate the defect site inside the stacked die. To allow this, the relation between the resulting phase shift and the penetrated layer thickness for each layer material has to be known.

3. Phase shift between different stacked die layers

First experiments using mold compound dummies were done determining the relationship between the penetrated mold thickness and the resulting phase shifts [7].

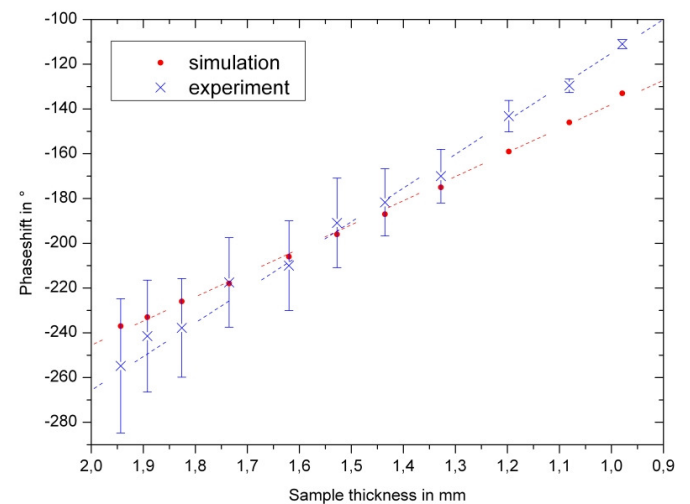


Figure 11: Experiment and simulation results taken from [7] in order to determine the defect depth related to the measured phase signal.

For further experiments a test sample with defined ohmic resistance and geometry was used. It consists of a stacked die built up with two identical meander-shaped test structures at each chip layer, shown in figure 12 in a sideview. The lower test structure is placed outside of the upper chip. In both cases heat flow is transferred only through the mold compound to the device surface.

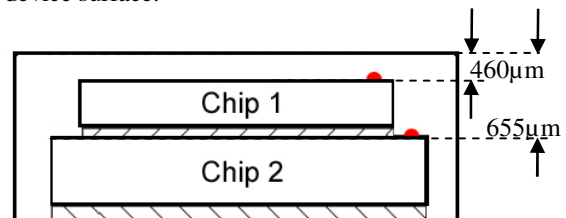


Figure 12: Side view of the device under test. The expected phase shift difference comes from the different depths of the defects (red points).

The meander-shaped structures have the same electrical behavior ($R \sim 93 \text{ Ohm}$) and were excited using a supply voltage of 0.18V. The current flow of 1.89mA leads to a power dissipation of 0.34mW. In order to allocate the LiT measurements the test sample was imaged by a X-ray inspection tool.. Figure 13 shows the resulting X-ray image and the position of the different chip layers from top side.

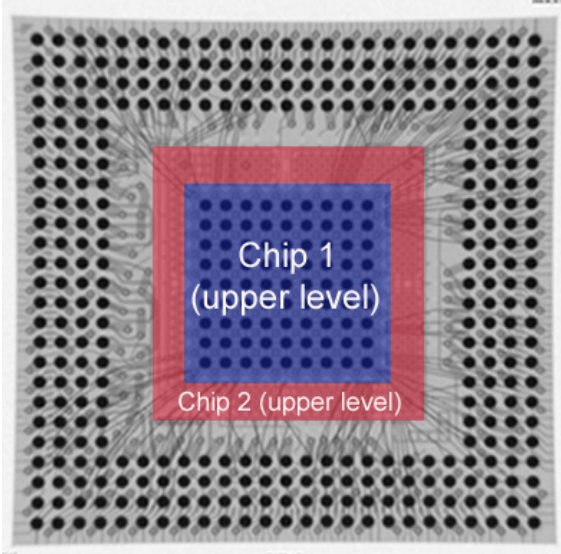


Figure 13: Top view of the test sample. The blue rectangle marks the dimension of the upper chip, the red one the chip below.

The heat generations of both test structures were measured using a lock in--frequency of 2Hz. To obtain a minimum required signal-to-noise-ratio the amount of measurement periods was increased up to 36,000.

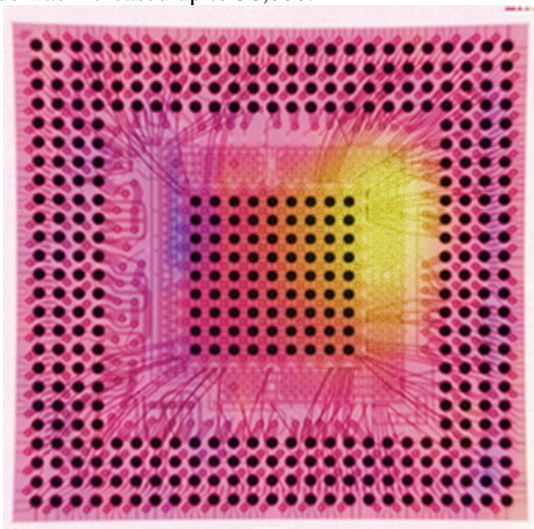


Figure 14: Overlay of X-ray and LiT-phase image of the upper test structure measured with a lock-in-frequency of 2Hz.

Linescans over both hot spots were taken to determine the phase signal. Own to the low signal- to-noise ratio both linescans were smoothed by a moving average-function allowing a determination of the required phase shift.

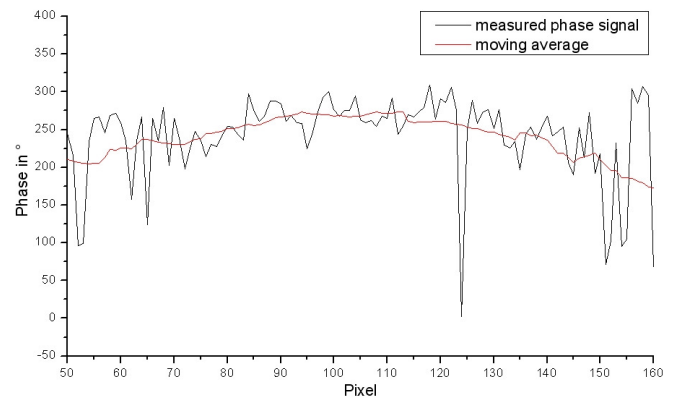


Figure 15: Linescan over hot spot occurring at the upper chip level including smoothing function.

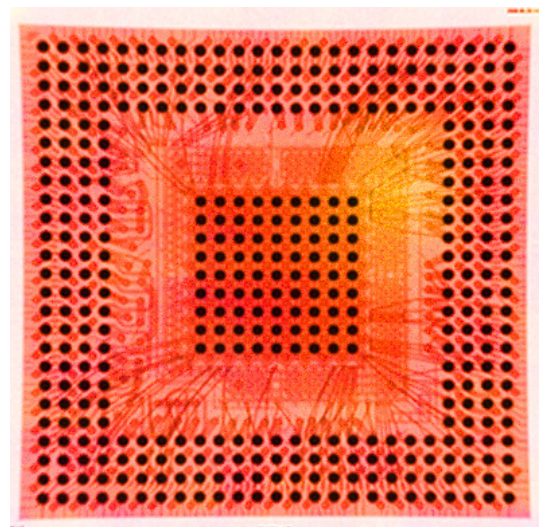


Figure 16: Overlay of X-ray and LiT-phase image of the lower test structure measured with a lock-in-frequency of 2Hz.

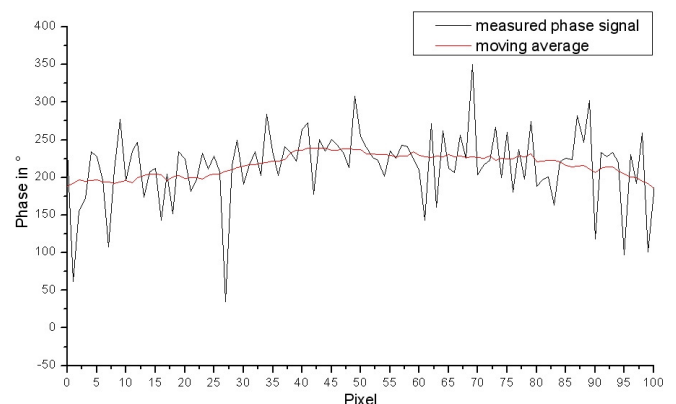


Figure 17: Linescan over hot spot occurring at the lower chip level including smoothing function.

For the upper chip level (Figure 15) a maximum phase of 273° was determined which is equivalent to a phase shift of 87° . For the defect on the lower chip level (Figure 17) the phase was measured with 239° which results in a phase shift of 121° . The phase shift difference caused by the known distance of $197\mu\text{m}$ between both chip levels amounts to 34° .

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Conclusions

LiT can be used for non-destructive defect localization in fully packaged devices. It was shown that inner hot spots occurring by ohmic shorts can be visualized and allocated at the device surface. In order to get an adequate signal to noise ratio at the device surface the lock in frequency has to be reduced to several Hz. Due to the low frequencies and the necessary heat flow through the mold compound thermal spreading leads to a reduction of lateral resolution of this method. For single chip devices or defects in the upper interconnect level of a multi chip device this can be improved by reducing the mold thickness above the defect by local grinding. For single chip devices with inner short paths LiT can be used to differentiate between chip- or interconnect-failures. Vertical localization of the short defect is helpful, if the mold thickness should be remained. For more complex multi chip devices vertically allocation of the defect in a non-destructive way can reduce the failure analysis flow significantly, and is one of only several methods allow defect localization without annihilating the overall functionality. For stacked die devices with separately connected chips an analysis flow was found to allocate the defect chip level. An all-encompassing method to allocate the defect vertically can be by measuring the phase shift of the thermal signal. It could be shown that the LiT is in principle able to allocate the defective chip level by measuring the phase shift. Additionally, the relationship between phase shift and mold thickness above the hot spot was determined in a previous work [7] and can be used to recalculate the defect depth.

Outlook

The heat transfer through multi layer systems has to be investigated to allow vertical defect allocation in complex multi chip devices. Each material layer like mold compound or die attach contributes a discrete value of phase shift which can be used recalculating the failure depth. Furthermore, the sensitivity of the LiT and analysis routines has to be improved to allow phase shift detection with a higher accuracy. Nevertheless, thermal simulations can be used as a comparison to experimental results and to predict the heat transfer through device.

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References

- [1] Reverdy, A., et al.: “3-D Defect Localization by Measurement and Modeling of the Dynamics of Heat Transport in Deep Sub-Micron Devices”, *Proc 33rd Int’l Symp for Testing and Failure Analysis*, San Jose, CA, November 2007
- [2] Khandekar, S., et al., *Liquid Crystal Microscopy*, Microelectronic Failure Analysis Desk Reference, Fourth Ed., (EDFAS 2002), pp.739-44
- [3] Hechtl, M. et al. „Localization of Electrical Shorts in Dies and Mold compounds using Magnetic Microscopy and Lock-in-IR-Thermography”
- [4] Breitenstein, O. et al., “Developments in IR Lock-in Thermography”, *Proc. 30th Int. Symp. for Testing and Failure Analysis, ASM Intern. Mat. Park, Ohio November 2004*, pp. 595-599
- [5] Breitenstein, et al., "Lock-in IR Microscopy with 1.4 μm Resolution by Using a Solid Immersion Lens", *Electronic Device Failure Analysis magazine* 8, 2006, pp.4-13
- [6] Breitenstein, O. et al., Microscopic lock in thermography investigation of leakage sites in integrated circuits, *Rev. of Scientific Instruments*, 71 (2000), 4155-4160
- [7] Schmidt, *et al.*, “ Application of Lock-in-Thermography for 3d defect localization in defect devices” *Proc 2nd Electronics System-Integration Technology Conference*, London, UK, September 2008, submitted